Amended Claims

2. (currently amended) A method of increasing the holding voltage of a LVTSCR structure that includes an n-well and a p-well formed in a substrate, an n+ and a p+ region formed in the n-well, and a n+ region formed in the p-well, the method [,] comprising forming at least one ~~additional p-region~~ p+ region and at least one additional n+ region ~~n-region~~ inside ~~a~~ the p-well of the structure to define ~~a~~ at least one p-n junction in the p-well that is forward biased during normal operation.

3. (currently amended) A method of increasing the holding voltage of a LVTSCR-~~like~~ structure having an anode in an n-well and a cathode in a p-well, comprising providing an alternative current path from anode to cathode through ~~a~~ the p-well of the structure, other than purely the current path from anode to cathode through the p-material of the p-well.

4. (original) A method of claim 3, wherein the alternative current path defines a lower resistance current path than the p-well.

5. (previously presented) A method of claim 4, wherein the lower resistance current path takes the form of at least one p-n junction that is forward biased under normal operating conditions, formed in the p-well.

6. (currently amended) A method of claim 4, wherein at least one diode is formed in the p-well which provides a low resistance current path through the at least one diode once the threshold voltage across the at least one diode is exceeded.